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Modified technique of using conventional slider boat for liquid phase epitaxy of silicon for solar cell application

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Abstract. **Epitaxial layers of silicon are grown on single crystal Si-substrate from a solution of silicon in indium using conventional graphite slider boat technique. The important problems of natural convection due to lower density of silicon compared to indium, poor wetting of substrate due to high angle of contact of indium solution on silicon substrate resulting in poor nucleation, melt removal from the growth substrate and saturation wafer associated with LPE in this technique are practically eliminated using sandwich method with simple modifications of the boat and the method of growth. Some experimental studies on the effect of different surface preparations of growth substrate are also reported. Growth results are shown and discussed. Further, improvization of slider boat to facilitate better study of growth parameters is suggested in the line of modification already carried out.**

Keywords. **Liquid phase epitaxy (LPE); silicon; slider boat; sandwich method.**

1. Introduction

Reduction of cost of solar cell is a need recognized globally. As the cost of amount of electronic grade silicon wafer used in a solar cell is a substantial fraction of its total cost, thin silicon solar cells fabricated on low cost substrates by an inexpensive method is an important goal in this line. Liquid phase epitaxy is an inexpensive method for silicon film deposition. Work on LPE growth of thin silicon film on single crystal Si, multicrystalline Si, upgraded metallurgical grade silicon, porous silicon, high temperature tolerant substrates like ceramics, low temperature substrates like glass for the purpose of solar cell fabrication are in progress in many laboratories all over the world. Some examples are the works reported by Astropower, USA (McNelly *et al* 1984); National Renewable Energy Laboratory (NREL), USA (Ciszek *et al* 1993; Wang and Ciszek 1994); Max Plank Institute (MPI), Stuttgart, Germany (Blakers *et al* 1992; Bergmann *et al* 1993; Konuma *et al* 1994a,b; Lee *et al* 1994); Institut fur Kristallzuchtung, Berlin and several other institutes in Germany (Steiner and Wagnor 1995; Wagnor *et al* 1997); University of New South Wales (UNSW), Sydney, Australia (Shi *et al* 1993; Zheng *et al* 1994), Australian National University (ANU), Canberra, Australia (Ballhorn *et al* 1998; Weber *et al* 1998), Cannon Inc., Japan (Nishida *et al* 2001); University of Konstanz, Konstanz, Germany (Peter *et al* 2002) and many other places. LPE layers are grown on single crystal silicon at first to study the properties of LPE layers and to optimize growth parameters for an LPE set up. In some cases, such layers are grown using epitaxial lateral overgrowth (ELO) technique (Suzuki *et al* 1990; Bergmann 1991). Weber *et al* (1998) detached such ELO epilayers grown on patterned substrates to study the properties of LPE layers more effectively in a method termed Epi-lift. Ultimate target of detachment of epilayer from Si substrate is fabrication of thin solar cells.

Conventional diffusion of the top surface of LPE layers may be carried out for junction formation. At MPI, Stuttgart, Blakers *et al* (1992) reported solar cell by phosphorus diffusion on 20 μm *p*-type LPE layer, which recorded open circuit voltage (V_{oc}) up to 663 mV, short circuit current density (J_{sc}), 27·5 mA/cm^2 and efficiency, 13·8%. At NREL, Ciszek *et al* (1993) reported solar cell on cast metallurgical grade multicrystalline silicon substrate with efficiency about 4% (V_{oc}, 536 mV). At ANU, Weber and Blakers (1995) reported 13·5% efficiency with V_{oc}, 612 mV, J_{sc}, 28 mA/cm^2 and fill factor (FF), 0·76 for solar cell on 35 μm LPE multicrystalline layer. LPE facilitates auto-doping of thin epitaxial layer and thereby introduces drift field in solar cell without any extra step (Bergmann *et al* 1993). Even there is report of junction formation at the time of LPE growth that produced open circuit voltage of 550 mV without front grid, surface passivation and antireflection coating (Bergmann *et al* 1993). After LPE growth on inactive highly doped Si-substrate and subsequent junction formation, sub-

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strate-thinning technique is applied to reduce thickness of the cell for higher efficiency (Zheng *et al* 1994). LPE layer on highly doped Si-substrate produces back surface field. This advantage combined to substrate-thinning technique was used to fabricate solar cells on LPE layers of efficiency up to 16·4% (Zheng *et al* 1996). Recently, Nishida *et al* (2001) reported solar cell on LPE grown layer on porous silicon substrate. Peter *et al* (2002) reported 9% efficiency (V_{oc}, 597 mV) for solar cell on LPE layer grown on upgraded metallurgical grade (UMG) silicon substrate.

Liquid phase epitaxy set ups are generally classified as per the type of boat used: horizontal slider boat (Dawson 1974; Lu *et al* 1992; Ogawa *et al* 1995), vertical dipping boat (Baliga 1977), tipping boat (Astle 1990; Weber and Blakers 1995) and automated centrifuge boat (Konuma *et al* 1993, 1994a) are the principal systems. Of these, horizontal slider boat system has been proved to be most popular and versatile (Astle 1990) and boat material considered to be best is graphite. However, this system has some problems, particularly for silicon LPE. Melt carry over and its removal from substrate surface (Zytkiewicz 1989), constitutional super cooling (Minden 1970) and nucleation difficulties (Sang and Miller 1970) are general problems. The first one arises from the fact that some melt seeps through the gap between substrate and slider when the melt is pushed or pulled. After cooling, that melt solidifies and sticks to substrate. Constitutional super cooling occurs due to a depletion of the liquidus temperature of the melt at the interface created by depletion of the solute during growth (Longo *et al* 1972). In addition to these there is a problem of natural convection, which is especially important to silicon epitaxy. Density of silicon at growth temperature is in the vicinity of 2·6 g cm^{-3} while that of melts are much higher, viz. for indium it is nearly 6·5 g cm^{-3}. When silicon saturated metal solution is cooled, the silicon, separated from the solution would flow upward due to buoyant forces and the substrate placed under the solution would not get silicon atoms for deposition. This problem of natural convection, referred to in the LPE literature as solutal convection, was recognized since early days of LPE (Long *et al* 1974) and the problem was discussed theoretically in LPE literature (Wilcox 1983). However, its extreme importance for silicon LPE was appreciated when Sukegawa *et al* (1988) developed a sandwich method in which the saturated melt was kept between two horizontal growth substrates, one placed above the saturated solution and another below it. The wafer placed below may act either as a source or as a growth substrate, while the one above acts as the growth substrate.

Most of other researchers of silicon LPE have either avoided horizontal slider boat or taken small amount of solvent metal. When thickness of melts remains within 2 mm, solutal convection effect remains under control (Astle 1990) for LPE growth of GaP under normal conditions. Similar result may follow for silicon LPE using indium melt. But using such thin solution has the problem that the metal melts form a drop on the substrate due to high surface tension. Then only one part of the wafer remains under solution and growth cannot occur at all parts. In addition, bad wetting of the growth substrate due to large angle of contact causes problem to nucleation. In this context, wetting includes interaction between solvent and any surface layers, e.g. oxides or adsorbed contaminants (McNelly *et al* 1984). It has been repeatedly pointed out in LPE literature that good wetting of growth substrate to the saturated melt is essential for nucleation and the problem associated with nucleation have been discussed (Wilcox 1974; McNelly *et al* 1984; Zinke-Allmang 1999). Use of weighted pistons on the growth solution (Long *et al* 1974) has been recommended to allow the solution spread. A sandwich method was proposed (Meinders 1974), where the melt was kept between lower growth substrate and an inactive plate over the melt to allow the melt better contact to the growth substrate and to exploit some other advantages. However, the sandwich method proposed by Sukegawa *et al* (1988) is different from the above method in basic ideas. In their arrangement the growth substrate would be placed above the solution. They showed from theoretical arguments (Kimura *et al* 1994, 1996) that sandwich method was best for silicon epitaxy. However, their work was done in special type of boats (Sukegawa *et al* 1988) from the very beginning. In the initial design of their boat melt could not be cleared from growth substrate after growth. This resulted in strain in the grown layer. Later, they redesigned their boat to make it suitable for melt removal (Kimura *et al* 1991; Kanai *et al* 1996). Here they used a much more elaborate arrangement with two pull rods. The arrangement needed better instrumentation and must have been costlier too. We, instead, improvised our simple slider boat LPE facility without any extra cost for the sandwich device and used only one pull rod as in the original boat instead of the two pull rods used by them. The use of single pull rod simplifies the system and reduces the chance of leakage. The lower substrate may be either a growth substrate or a source substrate. The melt would be cleared satisfactorily immediately after growth. In addition, our simple improvisation of the boat provides idea of further improvisation of boat to use it for better control and study of different growth parameters. This paper describes (a) some theoretical arguments regarding placement of growth substrate, (b) our basic LPE set-up with particular emphasis on the boat design, (c) some modifications of it to adapt the apparatus for sandwich method, (d) discussion of typical growth results obtained using sandwich method and (e) how the idea of improvisation of the boat presented here would be extended further for better and controlled study of different growth parameters.

2. Some theoretical arguments regarding placement of growth substrate

An indium solution saturated with silicon at a temperature below melting point of silicon has a uniform density along a vertical line. When the solution is slowly cooled, some silicon atoms will be separated from the solution and move under diffusion and gravity aided convection. While the motion due to diffusion will tend to carry them to all places of lower concentration, convection will tend to move them directly upwards as they are of much lower density compared to the solvent. This will cause a net upward flow and higher concentration of solute atoms near the upper substrate. This buoyancy-driven solutal convection may be studied mathematically assuming the solution to be incompressible and Newtonian fluid. Let, fluid velocity in the melt is $\vec{u}\,(u, \boldsymbol{n}, w)$. The flow will be governed by the continuity equation, the Navier–Stokes equation, the convection–diffusion equation for solute concentration, c and a linear equation relating melt density to solute concentration (Murray *et al* 1991):

$$\nabla \bullet \vec{u} = 0, \tag{1}$$

$$\frac{\partial \vec{u}}{\partial t} + (\vec{u} \bullet \nabla)\vec{u} = -\frac{\nabla p}{\boldsymbol{r}_0} + \boldsymbol{m}\nabla^2 \vec{u} + \frac{g\boldsymbol{r}}{\boldsymbol{r}_0}, \tag{2}$$

$$\frac{\partial c}{\partial t} + (\vec{u} \bullet \nabla)c = D\nabla^2 c, \tag{3}$$

$$\boldsymbol{r}_0 = \boldsymbol{r}_0[(1 - \boldsymbol{b}(c - c_0)], \tag{4}$$

where p is the fluid pressure, $\boldsymbol{m}$ the kinematic viscosity, $\boldsymbol{r}$ the density of the fluid, D the solute diffusion coefficient, $\boldsymbol{b}$ the solutal expansion coefficient, c the concentration of solute in the solution, subscripts zero representing values of the quantities at initial equilibrium state. In writing the equations, Boussinesq approximation is employed which assumes that density variation is important only in the body force term in the Navier–Stokes equations. The fluid parameters, $\boldsymbol{m}$, D and $\boldsymbol{b}$ are supposed to remain constant. Also, in writing the equations, velocity of the growth surface by virtue of growth is supposed to be negligibly small so that our reference frame attached to the planar crystal–melt surface is supposed to be at rest relative to the laboratory frame in which the velocity, $\vec{u}$ is measured.

These equations are to be considered along with the initial conditions

$$u = 0,\ p = 0,\ c = c_0 \text{ at } t = 0. \tag{5}$$

Boundary conditions on vertical walls will be

$$u = 0,\ \frac{\partial c}{\partial x} = 0 \tag{6}$$

and on the horizontal boundaries

$$u = 0 \text{ and } -\boldsymbol{r}D\left.\frac{\partial c}{\partial y}\right|_{y=0} = S_g, \tag{7}$$

where S_g is the concentration source term at the solution–substrate interface.

For diffusion-limited growth at slow cooling rate, the surface kinetics are fast enough to consider that mass transport is the only limiting factor for growth (Baliga 1986). But in this case, convection being dominant, interface kinetics become important rate limiting mechanism (Kimura *et al* 1994).

Assuming first order kinetics model (Ghez and Lew 1973; Kimura *et al* 1994, 1996), S_g may be given by

$$S_g = K\,(c_i - c_e), \tag{8}$$

where c_i and c_e represent interfacial and equilibrium concentration, respectively.

Assuming two-dimensional process, computer simulation of the above equations (Kimura *et al* 1996) predicts higher growth of the upper substrate for solution thickness > 2 mm. As the gap becomes wider, convection becomes more important and thickness of growth layer increases. Not only this, for wider substrate spacing the upper growth surface becomes smoother (Kimura *et al* 1996). So, while using the growth substrate above the solution there is no compulsion to take small amount of solution.

3. The basic apparatus

Our LPE set-up is a horizontal slider boat system. Many detailed descriptions of such systems are available in the literature (Lu *et al* 1992; Venkataraghavan *et al* 1999). Some of the important features of our system are described below in brief. The basic components of our LPE set-up are the following: (i) reactor cell: horizontal slider boat; (ii) furnace assembly; (iii) vacuum system; (iv) programmable temperature controllers and (v) gas flowing assembly and hydrogen purifier system.

Figure 1 shows photograph of the total LPE unit. Apart from the five basic units mentioned above, we fabricated a few more small units to facilitate our work. Those were a T-obstructer to improve push-pull arrangement, a weighted piston and stands for solution recovery. Also we modified the slider boat slightly with considerable benefit for LPE work.

3.1 *Reactor cell: horizontal slider boat*

It is a conventional slider boat, made of poco-graphite. Figure 2a shows the components of the slider units consisting of three slide-able parts. B and C can move along accurately designed channels grooved on the vertical sides of A. Figure 2b shows a vertical section along

length of the slider boat units as to be mounted for use. There are four rectangular grooves on B, each 2·5 cm square and of a depth of 0·125 cm relative to the surrounding graphite surface. It is desired that the substrates be placed in the grooves with appropriate spacers under those so that the clearances are suitable for melt removal. C is the solution containing well, both the top and bottom are open with four compartments, henceforth referred to as solution bins. The bottom openings of the bins are slightly smaller than the top openings as seen in vertical section of C (figure 2b). When C is placed on B using the upper channel grooved on the vertical side of A, its lower side become nearly closed by the surface of B. Measurements of base of each solution bin of C match with the grooves of B while all the components are mounted on channel. When needed, C could be pushed or pulled by an external push–pull rod arrangement to bring the solution(s) in contact with substrate.

3.2 *Furnace assembly, vacuum system, temperature controller and hydrogen purifier*

The furnace assembly consists of three coaxial quartz tubes and one helical heating coil placed coaxially between two inner tubes. Outer tube is gold coated, opaque at room temperature and nearly transparent at 800°C and above. The graphite boat is placed in the innermost tube, henceforth called process tube, of length nearly 86 cm and diameter, 7·5 cm. The intermediate tube protects the gold-coated tube from the heating element.

The vacuum system consists of a rotary pump and a diffusion pump. These are used to evacuate the system from the outlet end of the process tube. Appropriate gas lines are arranged for evacuating the system including the process tube at the beginning of operation.

EUROTHERM2408, programmable temperature controllers are used to regulate temperature of the two zones of the furnace at same or different values using the controller. Temperature may be measured and controlled at an accuracy of about 1°C.

For ultra-pure hydrogen (UPH), MATHESON$^{(R)}$ 8382 Hydrogen Purifier is used. Appropriate lines are arranged for feeding the purifier by IOLAR hydrogen gas, purging the reactor cell and the purifier system by nitrogen before and after flow of hydrogen to the reactor cell and to feed the reactor cell by UPH.

3.3 *T-obstructer to improve push–pull arrangement*

At the time of pushing or pulling the solution containing well C, sometimes the entire boat or the parts A and B slipped and reached the end of the process tube where it is tapered. The boat would not remain horizontal at that position and melt transfer from source to growth wafer and its removal from the Si wafer after growth would be difficult. We felt it necessary to make a device to eliminate chance of slipping the boat or its components inside the process tube. Accordingly, we used some broken pieces of quartz pull rod to assemble an obstructer. It looked like T and henceforth we call it T-obstructer. We placed the T-obstructer at the gas inlet end of the process tube during growth experiments. It prevented the motion of boat units A and B when C was pushed to carry melt from source wafer to growth wafer or from growth wafer to the next groove of B after completion of growth experiment.

3.4 *Weighted piston and stands for solution recovery*

To apply pressure on the solution so that it spread well and come in good contact with the wafer, a weighted piston was made. It was made of graphite and designed slightly smaller than upper openings and a little bigger than lower openings of solution bins of C. In many cases solution was not wiped out fully from source and growth wafers. So, we made suitable stands of graphite to hold

Figure 1. Photograph of the complete LPE unit.

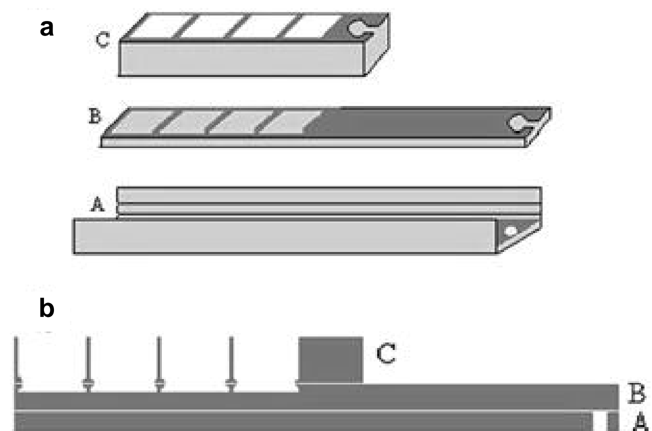

Figure 2. Horizontal slider boat for LPE: **a.** component units and **b.** vertical section (along length).

silicon wafers on those. The stands would be placed in the slider boat and silicon wafers with solidified melts sticking on those could be held vertically on those stands.

4. LPE growth experiments with growth substrate below the solution

LPE growth experiments and highlights of results with growth substrate below the solution are described below in outlines.

4.1 *Cleaning the substrate*

Silicon wafers were always cleaned by standard procedures using deionized water. Main steps of cleaning consisted of: (i) degreasing the wafer in acetone vapour, (ii) cleaning the wafers by ultrasonic vibrator, (iii) standard cleaning 1 [SC1] (Kern 1990; Beck 1998): heating the wafers in 5 : 1 : 1 :: H_2O : NH_4OH : H_2O_2 at 75–80°C for about 10 min and cooling the whole mass under flowing deionized water, (iv) standard cleaning 2 [SC2] (Kern 1990): heating the wafers in 6 : 1 : 1 :: H_2O : HCl : H_2O_2 at 75–80°C for about 10 min, washing and cooling in deionized water and (v) dipping the cleaned wafer in 10% HF solution for a few seconds just before loading to make it hydrophobic (Waber and Blakers 1995).

Slider boat units were baked in ultra pure hydrogen (UPH) ambient at processing temperature, nearly 960°C, for 3–4 h after each growth run.

4.2 *Choice of metal solvent*

Three different metal solvents were tried. At first copper with trace amount of aluminum was tried considering its various advantages as described in literature (Ciszek *et al* 1993), viz. (i) high solvent power of copper for silicon (about 0·05 wt% Si/°C near 940°C), (ii) low solid solubility of Cu in Si, (iii) easy gettering of copper from Si epilayer (Wang *et al* 1996) and (iv) minimal effect on resistivity of Si epilayer grown, because Cu is not a doping element.

However, we found that copper did not make good homogeneous solution with silicon at the process temperature our system could attain. Then, considering high solubility of silicon in aluminum (Girult *et al* 1977) and its effectiveness in removing thin oxide layers on growth substrates (Zopler and Barnett 1989), aluminum was tried. But we did not find it good either for homogeneous metal silicon solution or closed LPE layers. Finally, indium was considered due to its low melting point that helps in developing homogeneous solution and other factors mentioned in the literature (Shi *et al* 1996), viz. the silicon epilayers grown from indium melt (i) have better structural quality for photovoltaic application and (ii) at least as good electrical properties as layer grown from tin solution.

4.3 *Saturation of metal solvent*

First step in LPE growth experiment is saturation of the metal solvent by silicon. A piece of clean as cut ⟨100⟩ silicon wafer, called a source wafer, was taken in a groove of the slider boat unit B and the unit C was placed suitably to cover the wafer on which some measured amount of metal was placed. The whole boat assembly was then placed inside the process tube. The process tube was evacuated to about $2{\cdot}5 \times 10^{-4}$ torr and filled with UPH to atmospheric pressure and flow of UPH continued at 500 ml/min. Then the temperature of the furnace was raised in ramp at two stages. The melt was then saturated with silicon and baked at 960°C in UPH ambient for 3 h. Solubility of Si in indium at this temperature was about 2% atomic fraction (Girult *et al* 1977). The saturated solution was then transferred to the next groove of B by pushing the unit C. The system was then cooled to about 200°C in about 1–1·5 h, i.e. as quickly as possible under normal conditions. During cooling the dissolved silicon was separated from the solution, a part of which remained embedded in the solid lump and a small part was separated out.

4.4 *LPE growth experiment*

The next step was actual growth experiment. For this a source wafer and a growth wafer were cleaned. The solid solution of metal and silicon was washed in dilute HCl to remove any slag that might have come floating over it after baking. After HCl treatment it was repeatedly washed in deionized water and finally dried. To load the boat, the solid mass was placed over freshly cleaned surface of a source silicon wafer placed in first groove of slider unit B with both the units B and C mounted on A as seen in figure 2a. The process tube was again evacuated to $2{\cdot}5 \times 10^{-4}$ torr and then it was filled by UPH at atmospheric pressure. After this, flow of UPH through the process tube was continued at 500 ml/min and the furnace was heated to 960°C in two stages, in 45–60 min. At this position a dwell period of 2–3 h is needed to get a homogeneous solution of Si in indium. Despite the pre-saturation step described in § 4.3, this time is needed as the solid obtained after pre-saturation is effectively a rectangular block of indium with small pieces of silicon embedded in it. The pre-saturation step effectively allows one to get the lump of indium in a shape suitable for use in actual growth experiment and distribute pieces of silicon in the lump to speed up the formation of homogeneous solution during actual growth experiment.

Then the unit C was pushed to the next groove of B to carry the melt from source wafer to growth wafer. Once again the system was allowed to stabilize for about 30 min. Next step was cooling the system for growth of epilayer. The system was ramp cooled at different rates, typically at 0·3°C/min (or at higher rate up to 1·5°C/min). Final

temperature to end growth was also different (from 930–860°C). In some cases the ramp cooling started after slight etch back (Wang and Ciszek 1994; Shi *et al* 1995), i.e. increasing the temperature of the system by 3–5°C to allow any thin oxide layer to dissolve. After ramp cooling the system was kept in dwell for a short time (15–20 min) and then the solution bin C was pushed to next groove of B so that the melt would be removed from the growth wafer. The system was then ramp-cooled fast, to 200°C in about 1–1·5 h, maintaining flow of UPH. Of the different temperature profiles used, typical one is shown in figure 3.

It was desired that the melt wiped out from both source wafer and growth wafer in the process of pushing the melt to the successive grooves of B. But, almost invariably some solution leaked from the space between unit C and wafers placed on B. This solution remained on the wafers causing at least two problems: (i) growth continued at those places to make the growth surface rough at those points and (ii) finally the solution stuck on wafers. In case of traces of solution sticking on the wafers, HCl or other inorganic acids were used to clean the wafers. For small amount of solution sticking, however, surface roughness would not be too much. But, with larger amount of solution sticking on the wafers at various places, the surface would be rougher, as growth would continue at different areas for different lengths of time. Also, lengthy processes were to be followed to clean the wafers and to recover the solution. Those wafers were held nearly vertically in small graphite stands placed in the boat unit A. Then that unit was placed in the process tube, evacuated, filled with UPH and heated to about 300°C. Most of indium–silicon solution drained and the wafers were obtained nearly clean. Then HCl or Aqua Regia (HCl : HNO_3 :: 3 : 1) were used to remove traces of indium from silicon surface as suggested in the literature (Wang and Ciszek 1994). Thus poor melt clearance appeared to be a major drawback of this system of growth.

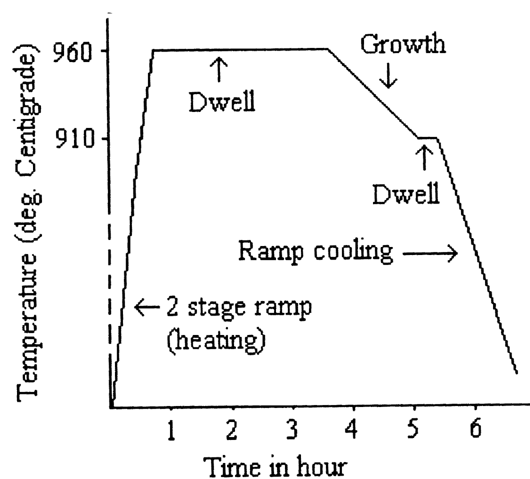

Figure 3. A typical temperature profile used in LPE growth experiments.

4.5 *Growth results*

Growth results were studied. Average epilayer thickness was estimated by gravimetric method. Epilayers of average thickness from 0 (no growth) to 5 μm were obtained in different growth experiments. Continuity of growth on the surface was studied by high power microscope (Carl Zeiss Jena) at 62·5 and 125 magnification and photomicrographs at different points were taken to record continuity of growth, nucleation and different phases of growth. Some SEM micrographs also were taken for the same purpose. But it was found that there was no good growth result. There were small areas where growth occurred. But some areas without any growth and some other areas where the silicon was dissolved surrounded most of those areas with LPE growth. We envisaged that it would be better to look for sandwich method suggested by Sukegawa *et al* (1988). But our system was not designed for sandwich method. So we started to look for improvisation of the method of work.

5. Improvisation of slider boat and its use for sandwich method of growth

Sandwich method refers to placing the Si-saturated metal melt between two growth wafers. At first we tried the method in the boat we had (Saha *et al* 2000) simply by placing another growth wafer on the metal solution and the weighted piston on that wafer. But there were several problems. Especially, the melt clearance was very poor. There was much better growth, but large amount of indium solution invariably stuck on the growth wafers, both upper and lower. Then a few simple modifications were done to the boat. A hole was drilled to the unit B (figure 2) in such a way that it came exactly above the hole on A when placed appropriately (figures 4a,b) over it (Majumdar *et al* 2001). Henceforth this new unit is called B̲ (figures 4a,b). A graphite bolt F (also shown in figures 4a,b) was such that it might be set in the two holes of B̲ and A to restrict the sliding possibility between

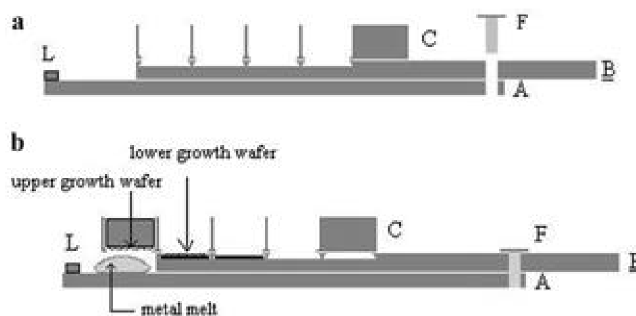

Figure 4. A vertical (longitudinal) section of the improvised boat **a.** components mounted at the time of loading (wafers, melt etc are not shown) and **b.** at the time of melt removal from growth wafers.

these two. When these two units were fixed, C could move freely from one end up to the position of the bolt. A small rod L of graphite of length nearly equal to that of the width of A, was used at the left end (as shown in figures 4a,b) of the boat component A to restrict motion of melt as described in the next section. With these modifications, LPE growth by sandwich method was done better and the melt removal was done more efficiently.

5.1 *Experimental technique used in the improvised slider boat*

To conduct LPE growth experiment by improvised boat, the wafers were cleaned in the method described in § 4.1. Also, pre-saturation of indium with silicon was done in the method similar to the one described in § 4·3. After cooling the saturated solution, an approximately rectangular piece of solid indium with pieces of silicon embedded in that was obtained as before. For growth experiment, one source wafer and two growth wafers, each as cut Cz *p*-type Si ⟨100⟩, of resistivity 2–3 ohm-cm were taken for cleaning. The source wafer and one growth wafer were of size $2{\cdot}5 \times 2{\cdot}4$ cm^2. The other growth wafer was slightly bigger, of size $2{\cdot}8 \times 2{\cdot}4$ cm^2. As mentioned before, the top openings of the solution bins of C were slightly bigger than the lower openings. The source wafer and the smaller growth wafer were taken in last two grooves of B̲. The solution bin C was placed over B̲ in such a way that the last bin of C came over the source wafer in B̲. Now the solid solution was taken in the last solution bin of C. Over the solid, the larger growth wafer was placed horizontally and then the weighted piston was placed over it. Neither of the upper growth wafer and the weighted piston would fall from the solution bin even after the metal melt was allowed to drain away as both were slightly larger than lower opening of the solution bin C.

After evacuation to about 3×10^{-4} torr, the process tube was filled by UPH and temperature of the furnace was increased keeping the flow of UPH unchanged as in the case of growth experiment (§ 4.4) with growth substrate below the melt. After ramp heating to about 960°C and dwell for about 2 to 3 h Si-saturated indium melt was obtained. This saturated melt (in unit C) was pushed to the next groove of B̲. Then two growth wafers one below and other above the melt formed the sandwich. After a dwell period or in some cases after slight etch back as in the case of growth with lower wafer only (§ 4.4), the system was ramp cooled for growth. Different temperature profiles were used (e.g. as shown in figure 3). After cooling to the desired level for growth (at 0·3°C/min–1·5°C/min as described in § 4.4), a short dwell was allowed. Then the solution bin was pushed forward to let the melt slip to the boat unit A. Then the tube was ramp cooled to about 200°C in about 1–1·5 h. Figure 4b shows a vertical section of the improvised boat unit at this configuration.

Melt clearance from the growth wafers was nearly perfect in this case. The upper growth wafer remained inside the solution bin in C, which now contained the weighted piston also. After overnight cooling, some traces of solid solution were found sometimes on either of the growth wafers or the source wafer. Those were removed in a method similar to the one followed in the case of growth with lower substrate only.

5.2 *Growth results in sandwich method with as cut growth substrate*

Growth results were studied for growth on both lower and upper substrates. As before (§ 4.5), average epilayer thickness was estimated by gravimetric method and continuity of growth on the surface was studied by high power microscope (Carl Zeiss Jena), photomicrographs at different points were taken to record continuity of growth, nucleation and different phases of growth. Some SEM micrographs also were taken for the same purpose. All the photomicrographs/SEM micrographs given here were obtained after one or other complete run. As would be seen below, different stages of growth were reached at different areas of the substrate at the end of a growth run, when fully closed layers were desired.

Three SEM micrographs of three growth areas on an as cut wafer are shown in figure 5. Nucleation is seen in figure 5a. But there is no closure of grown layer. This micrograph represents early termination of growth. Figure 5b shows an area of better growth. Figure 5c shows an area of still better growth. All these areas are seen in same growth wafer indicating termination of growth at different stages. In most of the growth wafers, these three types of areas are seen in different proportions.

5.3 *Discussion of growth results in sandwich method with as cut growth substrate*

We tried to locate the specific reasons behind this problem. It seemed that this might be due to growth of thin oxide layers on Si substrate surface that prohibit solvent contact (Donnelly and Milness 1966). Even after satisfactory HF dipping of the substrate just before loading, the possibility of growth of a few angstrom oxide layers during evacuation, hydrogen filling, preheating and saturation period cannot be ruled out (Bergmann and Kurianski 1993; Kunhle *et al* 1997). Also the aspect ratio, defined as the ratio of lateral growth width to thickness of epitaxial Si-layer, was only $\sqrt{2} : 1$ for partly oxidized ⟨100⟩ Si surface (Bergmann 1991; Bergmann and Kurianski 1993). Thus the possibility of epitaxial lateral overgrowth is also very poor. We did not use aluminum, following the observation of Bergmann and Kurianski (1993) that aluminum does not remove surface oxide layer uniformly and aids in opening localized hole only. Thus oxide growth appeared to be a major concern to us.

Other possibilities might be irregular number of nucleation sites on the as cut growth substrate due to difference in number of screw dislocation and mis-orientation at different points. It was found (Suzuki *et al* 1990) in the case of silicon LPE that growth does not occur unless there are screw dislocations or mis-oriented steps. As a reason behind it, it was suggested that the supersaturation is so low in solution growth that screw dislocations and mis-oriented surfaces supply most of the growth steps, rather than 2D nucleation (Nishinaga and Suzuki 1993). It was also pointed out that critically sized nuclei disappear while seeding crystals exceeding the critical grain size serve as nucleation sites (Wilcox 1974; Kunhle *et al* 1997). Other probable reason may be beginning of growth at different points at different times due to lack of identical contact of growth surface with silicon atoms separated from the solution.

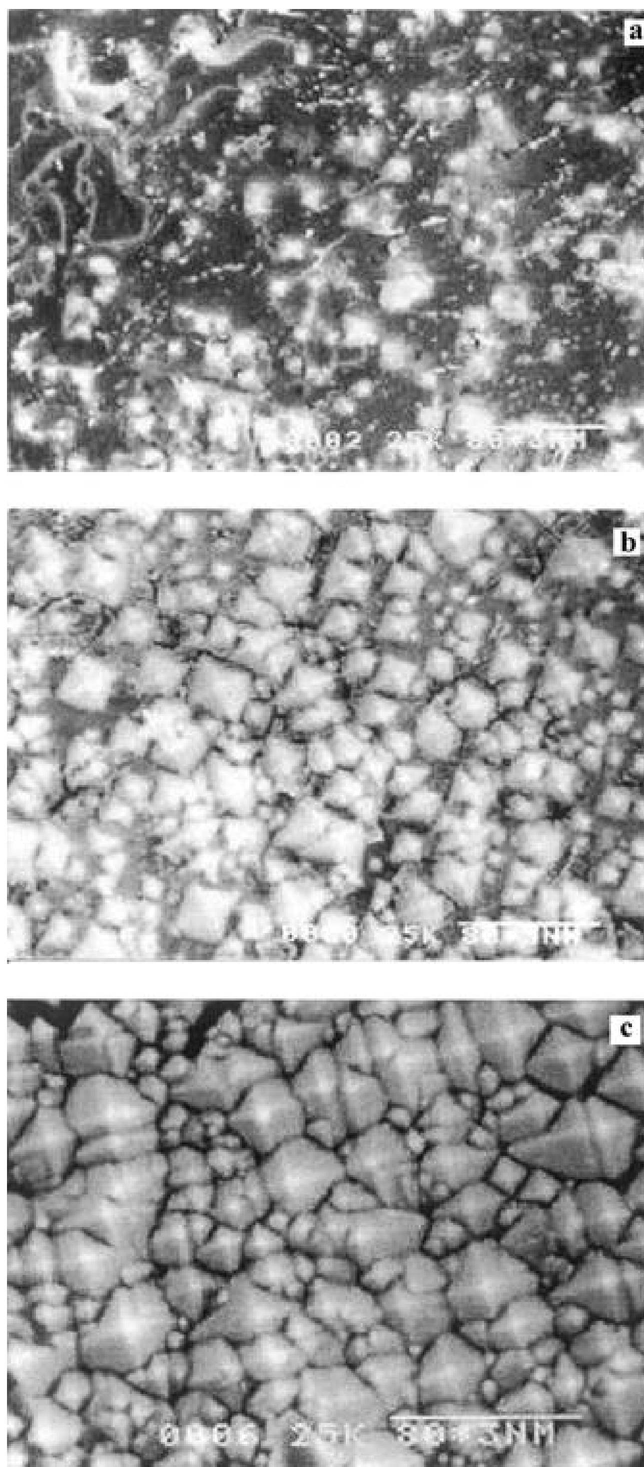

Figure 5. SEM micrograph of growth of silicon epilayer in improvised method on as cut silicon surface: **a.** an area where growth was terminated at an early stage, **b.** an area where growth terminated at an advanced stage and **c.** an area where good growth occurred.

We observed the problem early, just after a few growth runs. To attend the last possibility we arranged the weighted piston as described in § 3.4. In the sandwich method, the weighted piston would be placed satisfactorily (figure 4b). But the problem of patchy growth continued, albeit the better-grown areas of type of figures 5b and c increased. Also, with the new technique, continuous films of size up to about 1 cm^2 on growth substrate of $2{\cdot}5 \times 2{\cdot}5$ cm^2 were grown successfully.

6. Growth experiment with special preparation of growth substrates

Then we tried to look for better surface preparation to prevent growth of oxide, improve surface diffusion of growth atoms and increase the number of nucleation sites on the growth substrate (Chatterjee *et al* 2001). It was envisaged that suitable simple surface preparation like alkali-polishing or random texturization would help. It is known that alkali polished surface has small smooth blocks (actually surfaces of truncated pyramids) separated by borderlines of other such blocks and textured surfaces have small pyramids distributed all over the surface. It was envisaged that the borderlines of alkali-polished surface might suit for early nucleation and the smooth areas might be helpful for surface diffusion of growth atoms separated. In such case, the alkali polished surfaces would be of advantage for closed epilayer growth. On the other hand, the relative roughness of textured surface might not facilitate surface diffusion to that extent (compared to alkali polished surface), but it might have greater number of nucleation sites, which would help better nucleation and thereby leading to better growth.

6.1 *Preparation of growth substrates*

To alkali-polish silicon surface a *p*-type Cz Si ⟨100⟩ wafer is etched in 20% alkali solution at 80°C for 5/6 min. The resulting alkali polished surface has small smooth areas separated by borderlines of other such areas as seen in figure 6a. For random texturization alkali polished surface is etched for 45 min in 2–3% alkali solu-

tion with 10% isopropyl alcohol. The resulting textured surface has small pyramids distributed all over the surface as seen in figure 7a.

6.2 *Results of growth experiment with alkali polished and textured surfaces*

Alkali polished wafers were used both as upper and lower growth wafers. In many cases there were good nucleation at the edges of the smooth blocks of the alkali polished surface, but growth on the smooth blocks was not continuous (Chatterjee *et al* 2001). Photomicrographs of two different growth situations on such surface are shown in figures 6b and c. Figure 6b shows that growth started at the edges of the smooth blocks, but adequate lateral

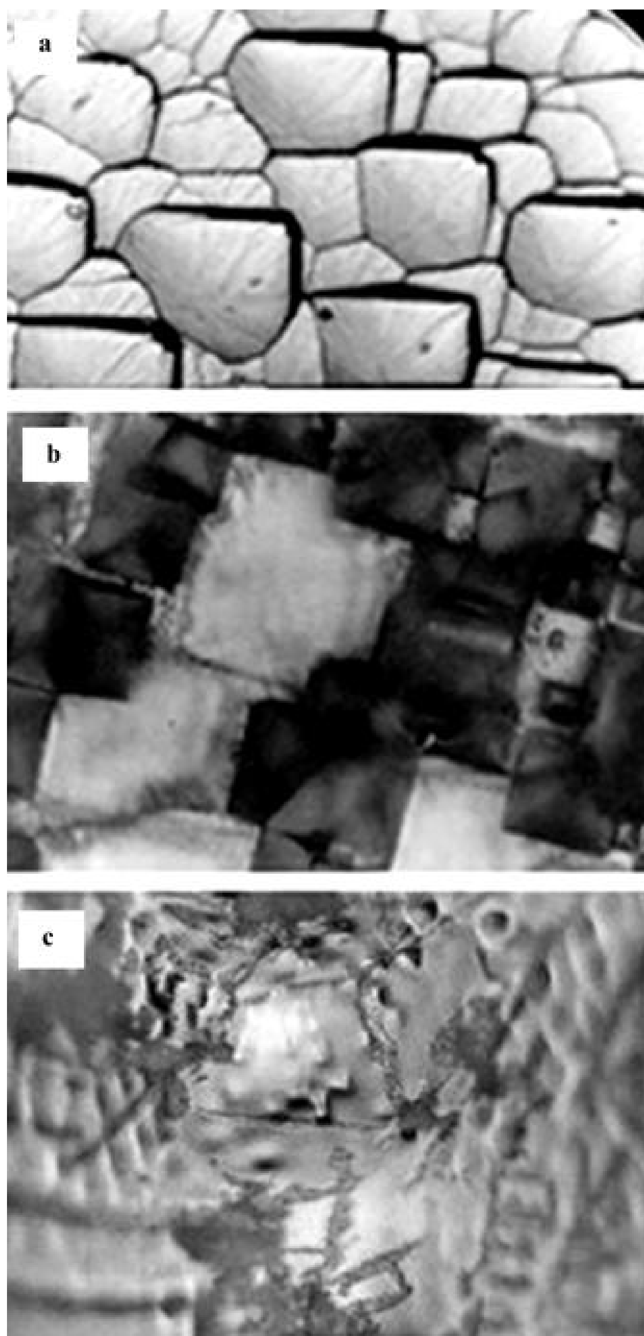

Figure 6. Photomicrographs of alkali polished surfaces: **a.** just after polishing, **b.** after growth run: growth occurred at the ridges, but no growth on smooth areas and **c.** after growth run: nucleation within the areas of dissolution.

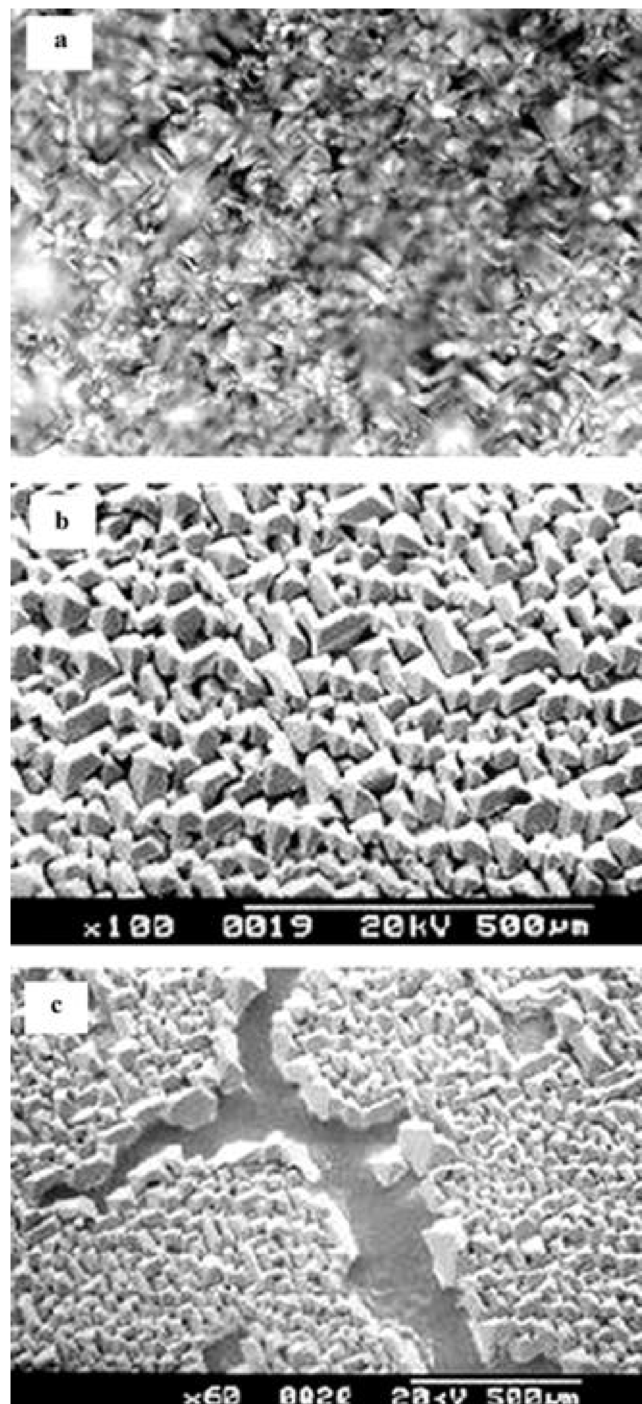

Figure 7. Micrographs of textured surfaces: **a.** photomicrograph of the surface just after random texturization, **b.** SEM after growth run: an area of good growth and **c.** SEM after growth run: an area where lateral overgrowth did not occur.

overgrowth did not occur. Figure 6c shows a spot on the lower wafer where silicon was dissolved and growth started at the ridges inside the groove formed by dissolution. Thus our expectation regarding nucleation was validated, but there was not adequate surface diffusion of separated atoms needed for lateral overgrowth on thin oxide layers that might have formed during evacuation, preheating and saturation stages.

Textured wafers also were used both as upper and lower growth wafers. Continuity of growth on textured wafers was much better in general. Continuous patches of grown layer of size around 0·5–1 cm^2 were obtained on the upper substrate. Figure 7b shows one such case of fairly good continuous growth. However, there were abrupt ends in the lateral growth on textured surfaces and full closed layers were not obtained. Typical discontinuities in growth layer are shown in figure 7c. Close examination showed that the termination of growth might be due to deposition of some slag on the growth substrate. This slag, likely to contain oxides of solute metal (Meinders 1974), was found to float and block contact of Si atoms arriving in the upper substrate at places. To remove such slag we washed the solid metal lump (with embedded silicon after pre-saturation) in dilute HCl just before loading for the actual growth experiment (vide § 4.4). But, we could not eliminate the slag completely. It seems a better optimization of the dilution of the acid and time of rinsing the metal block in it might be needed.

Some other probable reasons behind the problem are already discussed in § 5.3. It seems, addition of a small percentage of aluminum to the indium melt might be tried following the method of Wang *et al* (1996) for growth on multicrystalline substrate. Also the possibility of presence of relatively higher amount of water vapour and oxygen (Friedrich *et al* 1988) cannot be ruled out. Adsorbed water vapour in the boat and other surfaces in the growth system (Bergmann and Kurianski 1993) and leakages from o-rings, particularly at the position of pull rod might cause this problem. Finally, hydrocarbon related contamination problems from the high vacuum oil-pump are also probable. An oil-free diaphragm pump might be arranged to repeatedly rough pump the system after insertion of the wafers and prior to the growth (Bergmann and Kurianski 1993).

These steps will be undertaken in future to improve the quality and size of continuous epilayer. However, regarding the surface treatment, it seems appropriate to conclude that as cut Si ⟨100⟩ wafers or randomly textured Si ⟨100⟩ wafers are better as growth substrate compared to alkali etched Si ⟨100⟩ wafers.

7. Further improvisation of slider boat to facilitate study of epilayer growth

Following the improvisation of slider boat developed here further improvisation of slider boat has been proposed (Saha *et al* 2001) to facilitate study of epilayer growth by sandwich method. In this proposed improvisation of the slider boat, growth of four or six wafers or even larger number of wafers is possible at a time. That would make study of growth due to variation of growth parameters easier and more reliable. The main features of this boat are outlined in figures 8a,b. The unit A of the original boat is replaced by A_1 having two grooves M_1 and M_2. Two units, B_1 and B_2, have replaced unit B of the original boat. Each of B1 and B2 has two grooves, one for source wafer and the other for growth wafer. These are locked to A1 at the time of growth experiment by bolts H1 and H2. The new unit C1, in place of unit C of previous boat, has two triplets of solution bins. Initially, source wafer, melt and upper growth wafer are to be taken in S1 and S2. Lower growth wafers are to be taken on grooves G1 and G2 of B1 and B2. After saturation the unit C1 is to be moved so that two sandwiches are formed at G1 and G2 during growth. After growth, the unit C1 is moved further and melts fall at the grooves M1 and M2 of A1 as shown in figure 8b. The units B1 and

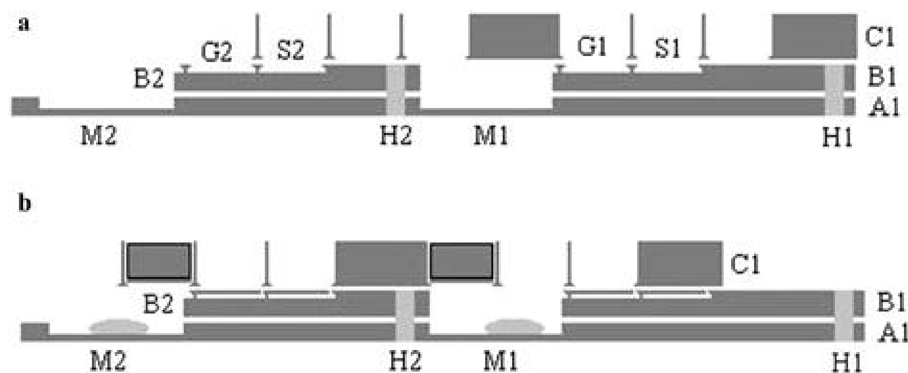

Figure 8. Vertical section of the units of proposed slider boat: **a.** as mounted at the time of loading in process tube (wafers, melt etc are not shown) and **b.** at the end of growth when melt was cleared from the wafers.

B2 may be more than two in number and the units A1 and C1 may be appropriately modified for simultaneous growth on more than two pairs of substrates. Different metal solutions, surface preparation of substrates, melt thickness might be taken in B_1 and B_2 keeping other growth parameters like ambient, temperature profile unchanged. Thus, a boat of this design might be used to study dependence of LPE growth on different parameters easily and more reliably.

8. Conclusions

An LPE set-up with slider boat reactor cell has been developed. Problems of growth of silicon epilayer keeping the growth wafer below silicon saturated metal solution and advantage of keeping the growth wafer above the metal solution has been discussed. The reactor cell has been suitably modified to keep growth wafer above metal solution and easy melt clearance after growth. Reasonably good quality epilayers have been grown over a surface area of about 1 cm^2. Different stages of growth were identified. As cut wafers, alkali etched wafers and randomly textured wafers were used. The growth has been more or less uniform at many places. Textured and as cut wafers show better uniformity and crystallite growth compared to alkali polished wafers. Growth of some slag appears to be a probable reason behind the termination of growth at an early stage at some places. A new slider boat with minimum cost escalation is suggested for better study of LPE growth process.

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References

Astle M G 1990 in *Liquid-phase epitaxial growth of III–V compound semiconductors* (Bristol: IOP Pub. Ltd.) pp 37, 42, 67

Baliga B J 1977 *J. Electrochem. Soc.* **124** 1627

Baliga B J 1986 in *Epitaxial silicon technology* (London: Academic Press Inc.) Ch. 3, pp 182–183

Ballhorn G, Weber K J, Armand S, Stocks M J and Blakers A W 1998 *Sol. Energy Mater. and Sol. Cells* **52** 61

Beck F 1998 *Integrated circuit failure analysis: A guide to preparation techniques* (West Sussex, England: John Wiley & Sons Ltd.) p. 52 (Translation: S S Wilson)

Bergmann R 1991 *J. Cryst. Growth* **110** 823

Bergmann R and Kurianski J 1993 *Mater. Letts* **17** 137

Bergmann R, Robinson S, Shi Z and Kurianski J 1993 *Sol. Energy Mater. and Sol. Cells* **31** 447

Blakers A W, Werner J H, Bauser E and Queisser H J 1992 *Appl. Phys. Lett.* **60** 2752

Chatterjee S, Majumdar D, Gangopadhyay U and Saha H 2001 *Characterization and defect studies of LPE layers of silicon grown on substrates undergoing various surface treatments, Crystal growth and characterization, Proc. int. workshop prep. & charac. tech. imp. single crystals* (eds) S K Gupta, S K Halder and G Bhagvannarayana (New Delhi: NPL) pp 532–536

Ciszek T F, Wang T H, Wu X, Burrows R W, Alleman J, Schwerdtfeger C R and Bekkedahl T 1993 *Conference record of 23rd IEEE PVSC* (Louisville: IEEE Electron Devices Society) p. 65

Dawson L R 1974 *J. Cryst. Growth* **27** 86

Donnelly P and Milness A G 1966 *J. Electrochem. Soc.* **113** 297

Friedrich J A, Neudeck G W and Liu S T 1988 *Appl. Phys. Lett.* **53** 2543

Ghez R and Lew L S 1973 *J. Cryst. Growth* **20** 273

Girult B, Chevrier F, Joullie A and Bougnot G 1977 *J. Cryst. Growth* **37** 169

Kanai H, Kimura M, Tanaka A and Sukegawa T 1996 *J. Cryst. Growth* **160** 229

Kern W 1990 *J. Electrochem. Soc.* **137** 1887

Kimura M, Tanaka A and Sukegawa T 1991 *Appl. Surf. Sci.* **48/49** 185

Kimura M, Dijilali N and Dost S 1994 *J. Cryst. Growth* **143** 334

Kimura M, Dijilali N, Dost S, Kanai H, Tanaka A and Sukegawa T 1996 *J. Cryst. Growth* **167** 516

Konuma M, Czech E, Silier I and Bauser E 1993 *Appl. Phys. Lett.* **63** 205

Konuma M, Hafendorfer M, Czech E, Silier I, Bauser E, Traxler A and Schweitzer G 1994a *Centrifuge for solution growth of semiconductor layers: An application of magnetic bearings, Proc. 4th int. symp. on magnetic bearings* (ETH Zurich: Vdf Hochsctru Verlag A Gander) pp 171–176

Konuma M, Silier I, Czech E and Bauser E 1994b *Sol. Energy Mater. and Sol. Cells* **34** 251

Kunhle J, Bergmann R B and Werner J H 1997 *J. Cryst. Growth* **173** 62

Lee S H, Bergmann R, Bauser E and Queisser H 1994 *Mater. Letts* **19** 1

Long S I, Ballantyne J M and Eastman L F 1974 *J. Cryst. Growth* **26** 13

Longo J T, Harris J S and Chu J C 1972 *J. Cryst. Growth* **15** 105

Lu Y C, Bauser E and Queisser H J 1992 *J. Cryst. Growth* **121** 566

Majumdar D, Chatterjee S, Gangopadhyay U and Saha H 2001 *Thin silicon solar cell on LPE grown layer in improvised slider boat, Crystal growth and characterization, Proc. int. workshop prep. & charac. tech. imp. single crystals* (eds) S K Gupta, S K Halder and G Bhagvannarayana (New Delhi: NPL) pp 640–644

McNelly J B, Hall R B, Barnett A M and Tiller W A 1984 *J. Cryst. Growth* **70** 420

Minden H T 1970 *J. Cryst. Growth* **6** 228

Meinders H 1974 *J. Cryst. Growth* **26** 180

Murray B T, Coriell S R and McFadden G B 1991 *J. Cryst. Growth* **110** 713

Nishinaga T and Suzuki T 1993 *J. Cryst. Growth* **128** 37

Nishida S, Nakagawa K, Iwane M, Iwasaki Y, Ukigo N, Mizutani M and Saoji T 2001 *Sol. Energy Mater. and Sol. Cells* **65** 525

Ogawa H, Guo Q and Ohta K 1995 *J. Cryst. Growth* **155** 193

Peter K, Kopecek R, Hotzel, Fath P, Butcher E, Zahedi C and Ferrazza F 2002 *Sol. Energy Mater. and Sol. Cells* **74** 219

Saha H, Majumdar D, Chatterjee S, Gangopadhyay U and Mondal A 2000 *LPE growth of silicon for photonic devices*, *Proc. int. conf. on fibre optics and photonics*, *Kolkata* (New Delhi: Allied publishers Ltd) pp 687–689

Saha H, Majumdar D, Chatterjee S and Gangopadhyay U 2001 Indian Patent application no. 482/cal/2001

Sang H and Miller W A 1970 *J. Cryst. Growth* **6** 303

Shi Z, Young T L, Zheng G F and Green M A 1993 *Sol. Energy Mater. and Sol. Cells* **31** 51

Shi Z, Zhang W, Zheng G F, Kurianski J, Green M A and Bergmann R 1995 *J. Cryst. Growth* **151** 278

Shi Z, Zhang W, Zheng G F, Chin V L, Stephen A, Green M A and Bergmann R 1996 *Sol. Energy Mater. and Sol. Cells* **41/42** 53

Steiner B and Wagnor B 1995 *J. Cryst. Growth* **146** 293

Sukegawa T, Kimura M and Tanaka A 1988 *J. Cryst. Growth* **92** 46

Suzuki Y, Nishinaga T and Sanada T 1990 *J. Cryst. Growth* **99** 229

Venkataraghavan R, Udayashankar N K, Rodrigues B V, Rao K S R K and Bhat H L 1999 *Bull. Mater. Sci.* **22** 133

Wagnor B, Wawra H, Dorsch W, Albrecht M, Krome R, Strunk H P, Riedel, Moller H J and Appel W 1997 *J. Cryst. Growth* **174** 680

Wang T H and Ciszek T F 1994 *Conference record of 1st IEEE world conference on photovoltaic energy conversion* (Hawaii: IEEE Electron Devices Society) p. 1250

Wang T H, Ciszek T F, Reddy R, Asher S and King D 1996 *Conference record of 25th IEEE PVSC* (Washington DC: IEEE Electron Devices Society) p. 689

Weber K J and Blakers A W 1995 *J. Cryst. Growth* **154** 54

Weber K J, Catchpole K and Blakers A W 1998 *J. Cryst. Growth* **186** 369

Wilcox W R 1974 *J. Cryst. Growth* **26** 153

Wilcox W R 1983 *J. Cryst. Growth* **65** 133

Zheng G F, Shi Z, Bergmann R, Dai X, Robinson S, Wang A, Kurianski J and Green M 1994 *Sol. Energy Mater. and Sol. Cells* **32** 129

Zheng G F, Zhang W, Shi Z, Gross M, Sproul A B, Wenham S R and Green M A 1996 *Sol. Energy Mater. and Sol. Cells* **40** 231

Zinke-Allmang M 1999 *Thin Solid Films* **346** 1

Zopler J C and Barnett A M 1989 *J. Appl. Phys.* **66** 210

Zytkiewicz Z R 1989 *J. Cryst. Growth* **94** 919